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Executive Summary

The main goal of the UPSIDE project is to use ultrasound stimulation for the treatment of depression, as an alternative to the much more intrusive solution of deep brain stimulation. Additionally, the project also includes research on neuronal recording signal decoding tools to identify depression biomarkers towards personalized therapy.

The ultrasound stimulation system is designed to be portable, requiring a power management unit (PMU) that converts a battery voltage into the different voltage levels required by the epidural-focused ultrasound device (eFUS) and the recording device (eREC).

In the planned work packages of the UPSIDE project, the design of the PMU was planned in Work Package 1 (WP1) and it is the responsibility of Silicongate Lda, with the help of TUDelft, to specify its blocks and architecture. TUDelft, with a system-level perspective, identified the required power domains and respective current requirements. SiliconGate, proposed a PMU architecture with five low dropout linear regulators (LDO), one boost DCDC converter and one analog-to-digital (ADC) converter for temperature monitoring.

After specification and architecture definition, the design phase was initiated. As one of the power domains (boost DCDC) requires a current level too high to be achieved with one single chip, due to power dissipation concerns and fabrication costs, the system was designed to be modular. Therefore, in order to achieve the target current capabilities, several PMUs can be combined in the PCB. Targeting the original specifications, 4 PMUs will be used, 1 in master mode (mode A) and the other 3 in slave mode (mode B). PMUs in slave mode have several blocks disabled, keeping active only the blocks required for the operation of the boost DCDC.

By the end of this first year of the UPSIDE project, the PMU was validated both in Verilog and with Simulation Program with Integrated Circuit Emphasis (SPICE) simulation and its layout was taped out. The prototype was sent for production in TSMC 180nm BCD technology using MUSE services.

Currently, the characterization test is being prepared while SiliconGate waits for the PMU prototype chips to arrive in the end of November 2023.