Grant Agreement No.	101070931
Start date of Project	01 September 2022
Duration of the Project	48 months
Deliverable name	**D1.4: CMOS recording interface with ~64 channels for EEG recording and passive MEAs**
Partner Leader	TUD
Dissemination Level	PU

Status	Final
Version	V1.0
Submission Date	28-2-2024

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History of Changes

Version	Change made	Date
V0.1	First Draft by XH	9-2-2024
V0.2	Review by DM – Updated by XH	19-2-2024
V0.3	Review by TC	19-2-2024
V1.0	Final by DM	20-2-2024

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UPSIDE Website: https://project-upside.eu

Abbreviations

ADC: Analog to Digital Converter

AFE: Analog Front-End

FUS: Focused Ultrasound

uECoG: Micro-ElectroCorticography

CMRR: Common-Mode Rejection Ratio

DBE: Digital Back-End

DRC: Design Rule Checker

EBI: Epidural Brain Interface

eFUS: Epidural Focused Ultrasound Device

eREC: Epidural EEG Recording Device

EDO: Electrode DC Offset

WP: Work Package

SPICE: Simulation Program with Integrated Circuit Emphasis

TSMC: Taiwan Semiconductor Manufacturing company

PCB: Printed Circuit Board

PMU: Power Management Unit

PEX: Parasitic Extraction

PLV: Phase Locking Value

PAC: Phase-Amplitude Coupling

PSRR: Power Supply Rejection Ratio

LUT: Look-Up Table

LVS: Layout Versus Schematic

MIM: Metal-Insulator-Metal

MOM: Metal-Oxide-Metal

P&R: Place and Route

PDK: Physical Design Kit

RTL: Register Transfer Level

SPI: Serial Peripheral Interface

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Executive Summary

The UPSIDE project has the overall goal of combining electrical recording and ultrasound stimulation for the treatment of depression, as a less invasive alternative to the more intrusive approach of deep brain stimulation.

The overall system is designed to be portable, with the core consisting of an epidural focused ultrasound stimulation device (eFUS) and a high-density epidural electrical recording device (eREC). This will allow for FUS stimulation of different brain regions and micro-electrocorticography (uECOG) readout of biomarkers in behavior experiments with animal models featuring depression-like symptoms.

In the planned work packages of the UPSIDE project, the design of the eREC was planned in Work Package 1 (WP1) and it is the responsibility of TU Delft. TU Delft, from a system level perspective, identified the specifications of the eREC, such as power, area, noise, channel count, etc. After specification definition, the design phase was initiated. A recording architecture has been proposed, focusing on minimizing both component footprint and power consumption. As a proof of concept, the WP1 will involve designing a prototype with 64 channels. The system is designed to be modular, such that it can easily be scaled to 1024 channels in the second phase of the project.

By the end of Q2/2024, the eREC will be validated using Simulation Program with Integrated Circuit Emphasis (SPICE) simulation and its layout will be sent for production in TSMC 40-nm 1p7m CMOS technology. TU Delft expects to receive the prototype eREC chips in August 2024 and start the experimental verification immediately, including *in vitro*, and *in vivo* validation.

1. Introduction

The UPSIDE project aims to develop radically new technology to interface with the brain by largely overcoming existing bottlenecks in brain recording and stimulation, such as the intrusive solution of deep brain stimulation. With experts in microelectronics, microfabrication and material science, signal processing, neuroscience and neurobiology, and focused ultrasound, the community gathers all the necessary expertise to take on this challenge and develop the next generation of brain implants.

The overall system is an epidural brain interface (EBI) designed to operate bidirectionally ("reading" and "writing"), requiring an epidural uECoG recording device (eREC) and an epidural focused ultrasound stimulation device (eFUS). A power management unit (PMU) converts a battery voltage into the different voltage levels required by the eREC and eFUS.

Fig. 1: Proposed epidural brain-interface (EBI): epidural focused ultrasound for stimulation (eFUS, green), epidural neural recording arrays (eREC, yellow). Closed-loop FUS stimulation is controlled by biomarkers detected in uECoG.

In the planned work packages of the UPSIDE project, the design of the eREC was planned in WP1, and it is the responsibility of TU Delft to define a suitable architecture and identify the required blocks, targeting a small footprint and low power consumption. The required other blocks for testing, configuration, and debugging purposes are specified as well.

Following the definition of specifications for both the eREC architecture and each individual block, the design phase was initiated. To ensure seamless integration with the eFUS and PMU during the final in-vivo validation, in-depth evaluations of the eREC alone will firstly be performed. These evaluations include both electrical characterization and *in vitro* and *in vivo* validations utilizing passive 64-channel uECoG arrays. Each characterization or experiment necessitates the development of a different setup.

The remaining sections of this report are organized as follows: Section 2 presents the eREC high-level architecture and specifications; Section 3 presents three different systems or setups that will be designed for the eREC characterizations and its final *in vivo* validations with the eFUS and PMU devices; Section 4 presents block-level design of the eREC, including both the analog front-end and digital back-end, serial peripheral interface (SPI), register map, as well as other aspects, including validation methodology, layout and packaging; finally, conclusions are drawn in Section 5.
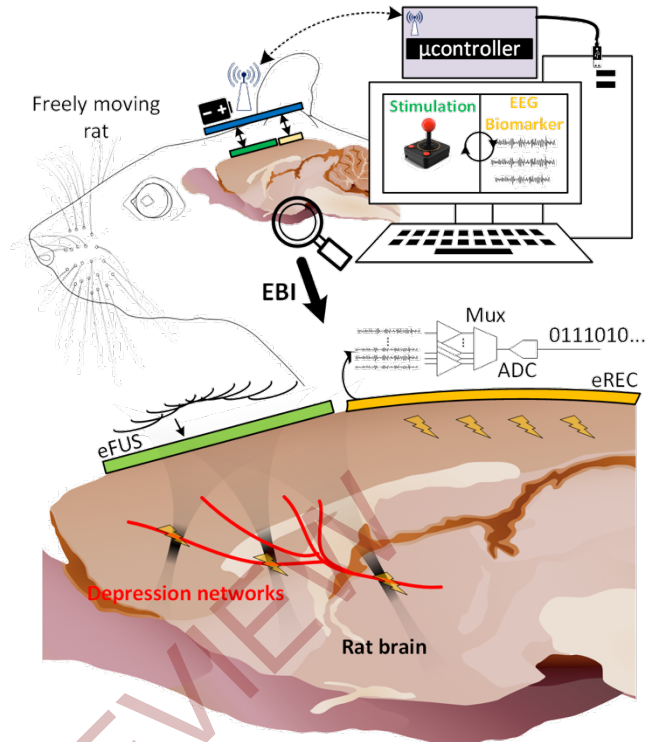
2. eREC Specifications
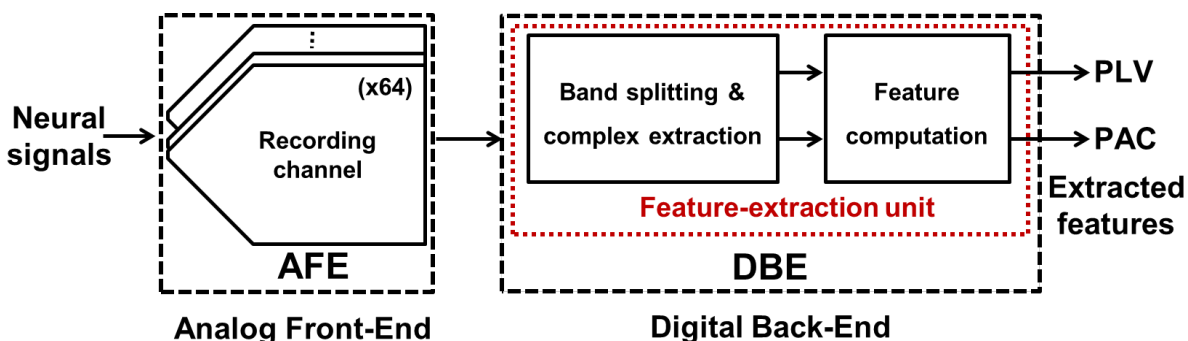
The eREC schematic is shown in **Fig. 2**.

Fig. 2: eREC simplified block diagram.

The AFE serves as the interface between electrodes and digital processing unit. It is responsible for filtering, signal conditioning, amplification, analog-to-digital conversion (ADC), etc. Essentially, the AFE digitizes the weak (µV-level) neural signals from the cortical surface, while rejecting large electrode DC offsets (EDOs), which can be up to tens or hundreds of mV.

On the other hand, the DBE processes the digitized neural signals received from the AFE, involving tasks such as filtering, decimation, feature extraction, etc. It plays a crucial role in interpreting the data from the digitized brain signals and deriving meaningful insights or facilitating actions, such as stimulation using focused ultrasound.

The eREC target specifications, including the analog front-end (AFE) and digital back-end (DBE), are specified and listed in Table 1.

AFE (analog front-end)

PARAMETER	SYMBOL	SPEC	UNIT
Channel count	N_{CH}	64	--
Area per channel	A_{CH}	<0.004	mm^2
Power per channel	P_{CH}	<2	µW
Signal bandwidth	BW	1-500	Hz
Input-referred noise	IRN	<5	$µV_{rms}$
Linear input range	IR	>3	mV_{pp}
Common-mode rejection ratio	CMRR	>40	dB
Input impedance	Z_{in}	>100M @1Hz	Ω
Input DC current	$I_{in,DC}$	<1n	A

Temperature	Temp	37	°C
Core power supply	AVDD	1.1	V
I/O power supply	VDDIO	3.3	V

DBE (digital back-end)			
Channel count	N_{CHD}	64	--
Area per channel	A_{CHD}	<0.015	mm^2
Power per channel	P_{CHD}	<1.5	µW
Core supply voltage	DVDD	1.1	V
I/O supply voltage	VDDIO	3.3	V

Table 1: eREC specifications

By defining these specifications as listed in Table 1, we define a clear reference point for the design and implementation of the eREC. Several critical specifications, including power, area, and noise, serve as targets or benchmarks that we aim to achieve in order to remain competitive with the latest advancements in the fields of neural recording interfaces. Furthermore, meeting these critical specs ensures that the eREC can operate properly within our application context, delivering accurate and reliable performance.

3. System Design

The system development for the eREC characterization setups occurs incrementally and involves three stages with three distinct setups (or systems) indicated as S1, S2, and S3. Each stage marks a significant progression, with specified functionalities and features tested and verified. This incremental development strategy allows for a structured characterization of the eREC device, ensuring that each subsequent stage builds upon the success and insights gained from previous stages. A brief overview of the three stages is provided below.

- S1 – Basic electrical characterization of eREC;

- S2 – Recordings *in vitro* and *in vivo* using 64-electrode passive ECoG arrays (i.e. without the inclusion of eFUS);

- S3 – *In vivo* recordings with focused ultrasound stimulation (i.e. system-level integration of eREC and eFUS).

System S1

System S1 marks the initial phase of eREC characterizations, represented by basic functionalities and performance metrics, including crucial aspects such as power consumption, linear input range, input-

referred noise, linearity, input impedance, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), etc. For this reason, system S1 will be relatively bulky in order to provide full flexibility during testing.

The focus is on ensuring the reliability and basic functionality of the eREC device. Power consumption is critical and the system need to operate within the specified power budgets while delivering reliable and accurate performance. Furthermore, noise will be carefully evaluated to minimize any potential interference and maintain good signal integrity, which is very important for this application as noise may easily degrade the overall system performance.

Linearity or distortion, another critical parameter, sets the accuracy of the eREC in response to input signals across a range amplitudes (linear input range). A low degree of distortion is essential for accurate digitization and faithful representation of the input neural signals.

A high input impedance ensures efficient signal transfer and minimizes signal attenuation and DC current flow.

CMRR and PSRR denote the system's ability to reject any fluctuations in common-mode signals and power supplies, which are crucial for maintaining stable performance in the presence of external disturbances.

Finally, fast artifact recovery, is another feature we aim to demonstrate. The ability to quickly recover from large artifacts, which can be induced by stimulation or movement, enhances the overall system robustness, making it highly desirable for any practical applications.

System S1 will be designed and manufactured at the beginning of Q3/2024 after the eREC chip is finalized.

System S2

Following the eREC electrical characterizations, we will perform *in vitro* measurements in combination with a 64-channel ECoG array dipped in a saline solution. Firstly, the noise of the complete readout chain (ECoG array plus eREC) will be evaluated with the saline solution grounded.

Subsequently, pre-recorded ECoG signals will be applied to the saline, and the eREC device will capture the resulting electrical activity. This step aims to validate the eREC's ability to accurately record neural signals in a simulated physiological environment. After these preliminary verifications, we will proceed to validate the eREC device *in vivo* in a practical biological setup.

During the *in vivo* validations, an ECoG array will be surgically implanted epidurally over the cortex of a mouse, closely mimicking real-life scenarios and allow us to evaluate overall system's performance in a live animal. Both time-domain waveforms and frequency-domain spectrogram will be analyzed from the recorded *in vivo* data to assess the fidelity and reliability of the recordings. These validations are essential steps towards ensuring the effectiveness and reliability of the eREC device for its final integration with the eFUS device.

System S2 will be designed based on the openephys headstage and the connector strategy used by Ghent University, as described in the periodic report of UPSIDE for year 1. The Intan chip used by Ghent University will be replaced with the eREC chip. This PCB was previously used to validate the uECoG electrode array by Ghent University.
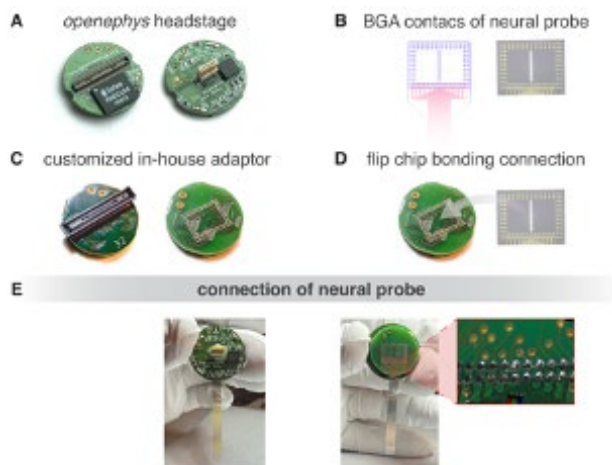
Fig. 3: Openephys headstage device to be modified for System S2.

System S3

Finally, in system S3, our goal is to validate *in vivo* the hybridization of the eREC and eFUS devices. By bridging the capabilities of eREC, which facilitates high-density neural recording and biomarker extraction, and eFUS, which delivers targeted focused ultrasound stimulation, this system will enable behavioral experiments involving animal models exhibiting depression-like symptoms, paving the way for more effective treatments and improved patient outcomes.

System S3 is planned in the activities of WP3 and will be defined based on the results from WP1 and WP2.
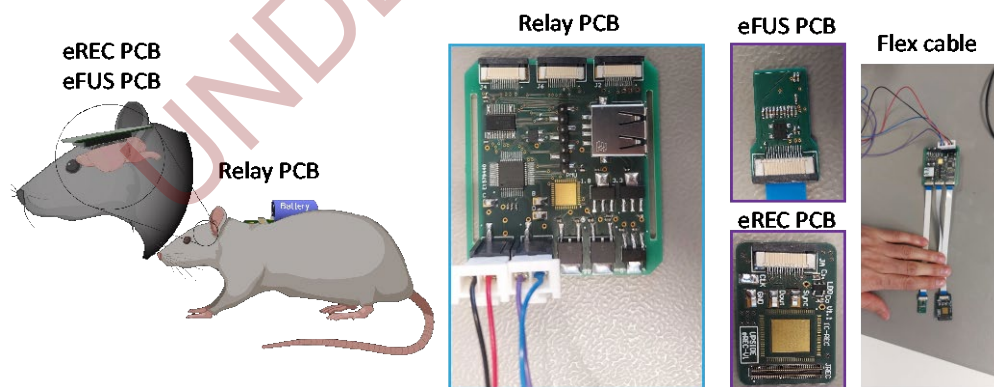

Fig. 4: System S3 for in vivo validations of the eREC and eFUS devices.

The first version of the system is currently being designed - see **Fig. 4**. The system consists of a relay PCB in the back of the animal that provides power and data communication to two small PCBs for eREC and eFUS through a set of flexible cables. More details about the system S3 is provided in the report for the deliverable D3.1.

4. eREC Block-Level Design

Following the system design, this section delves into the block-level design of the eREC, mainly including the analog front-end (AFE) and the digital back-end (DBE). A simplified block diagram of the eREC chip is shown in **Fig. 5**. The AFE incorporates 64 recording channels, whereas the DBE integrates two feature-extraction units. Additionally, other digital blocks, such as data serializer for transmitting the ADC data off-chip and SPI interface for eREC configuration, will also be described.

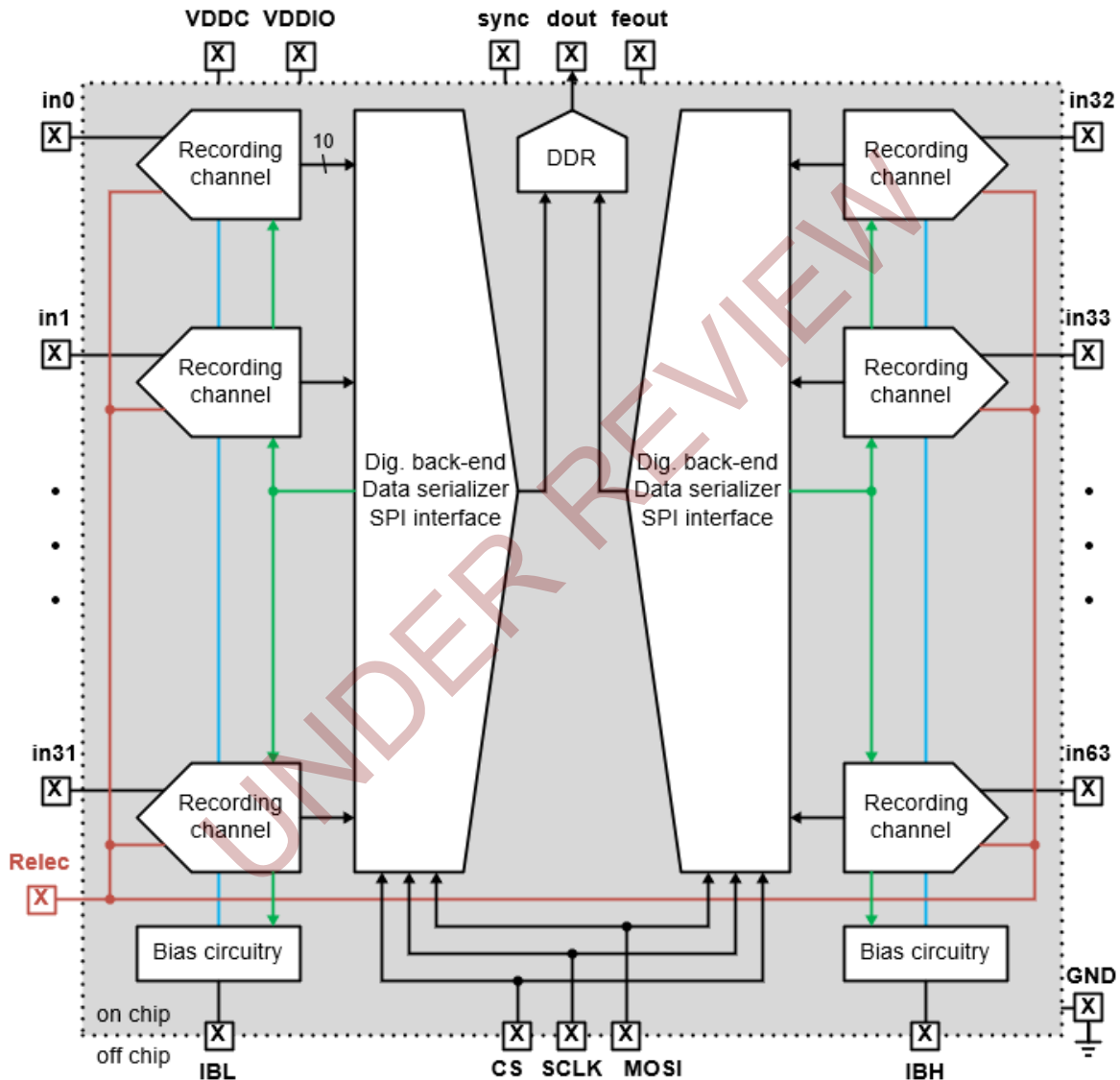**Fig. 5**: eREC simplified block diagram.

The recording channel architecture has been carefully chosen with the goal of minimizing both area utilization and power consumption while maintaining good performance (low noise and distortion levels).

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Regarding the input structure, AC-coupling is employed to reject rail-to-rail electrode DC offsets (EDOs) without any complex feedback loops and achieve a high input impedance, thus minimizing signal attenuation and current flow between brain tissue and recording electronics. While AC-coupling may require a large area, this can be mitigated by placing the input capacitors, implemented using metal-insulator-metal (MIM) or metal-oxide-metal (MOM) devices, on top of the active circuits partially or completely, depending on the available number of metal layers. A novel input biasing network has been proposed to avoid the disadvantages of commonly used pseudo-resistor elements in AC-coupled structures. This network has the ability to record neural signals at very low frequencies (<1 Hz, see **Fig. 10**) while also achieving fast recovery from large artifacts, which can be due to stimulation or motion.

The channel core utilizes an area-efficient approach of direct digitization with oversampled ADCs, as extensively demonstrated in recent literature [1-5]. Additionally, when operating in incremental mode, the digital decimation filter is highly efficient in terms of both power consumption and area utilization. Finally, a scaled CMOS technology can be employed to leverage power and area scaling benefits. Hence, we believe that an architecture that combines AC-coupling with direct digitization (in incremental mode, specifically incremental ADC), implemented in a scaled technology node, would be most suitable for this application. Such a scheme with its simplified block diagram is shown in **Fig. 6**. A schematic of the front-end OTA is also shown (see **Fig. 7**).
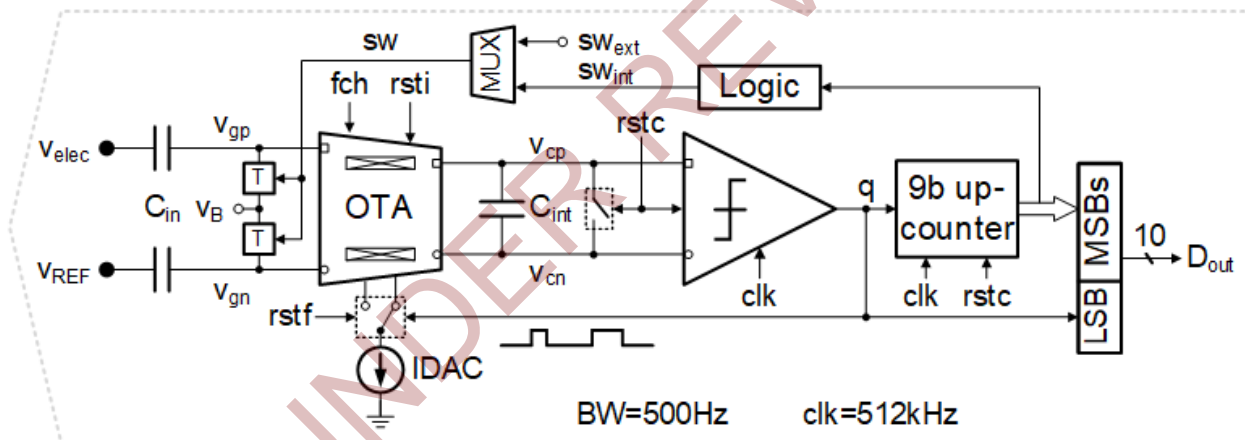

Fig. 6: Recording channel block diagram.

DBE – Feature-extraction unit

The digital back-end performs feature extraction on the raw data received from the recording channels. The goal is to extract generalizable features that could be applied to various algorithms with minimal area and power. These features can be directly used to drive the stimulation or as a pre-processing step to reduce the complexity of the neural signal classifier driving the stimulation.
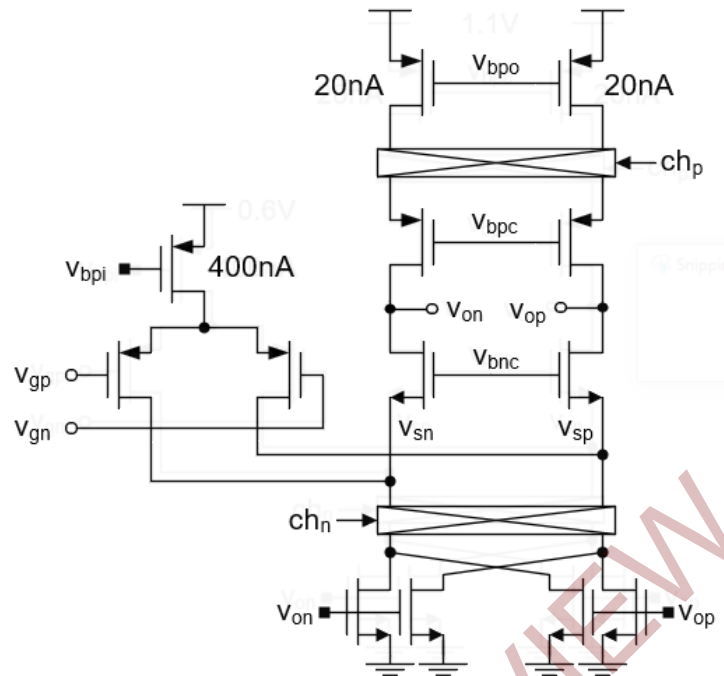
Fig. 7: OTA transistor-level schematic.

Neural recordings can capture oscillatory synchronization features to perform precise closed-loop neuro-modulation. Phase locking value (PLV) and phase-amplitude coupling (PAC) are commonly used features to quantify oscillatory synchronization. The first step to calculate PLV and PAC is to divide the raw data into different frequency bands and obtain the complex representation for each band. The energy per band can also be used as a feature. Typically, band splitting is achieved using Morlet convolutions, or a bandpass filter bank followed by Hilbert transforms. Both methods are inefficient when implemented in hardware. We proposed a new power-efficient multiplier-less wavelet approximation (the Hoda wavelet) and combine it with a multi-rate lowpass filter (LPF) bank for complex signal extraction. The next step to calculate PLV and PAC is to extract phase and magnitude from the complex signals. CORDIC processors perform accurate extraction at the cost of power and area efficiency. Low power approximations trade off accuracy with efficiency, but still require trigonometric lookup tables (LUTs) to implement the sine and cosine functions needed for calculating PAC and PLV. We developed a PLV/PAC unit that approximates the sine and cosine of the phase (or phase difference) directly from the complex signals, avoiding the complexity of phase extraction and trigonometric LUTs.
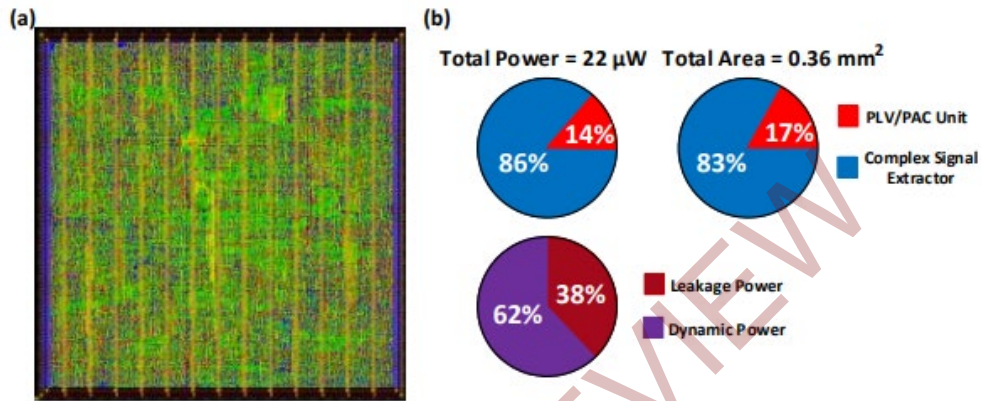
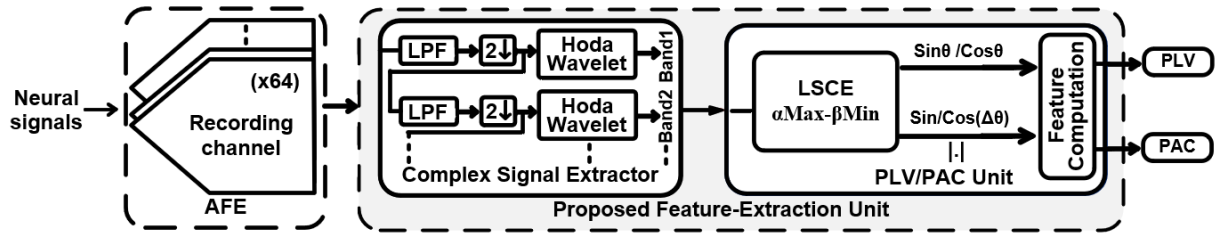**Fig. 8:** Digital back-end block diagram (top), and its layout view (bottom left) and power area breakdowns.

Designed in TSMC 40nm CMOS technology, our proposed feature extraction unit achieves 688 nW/channel and 0.011 mm^2/channel while maintaining good accuracy, which is a 2.5× and 5× improvement over the state-of-the-art in power and area efficiency [6-7].
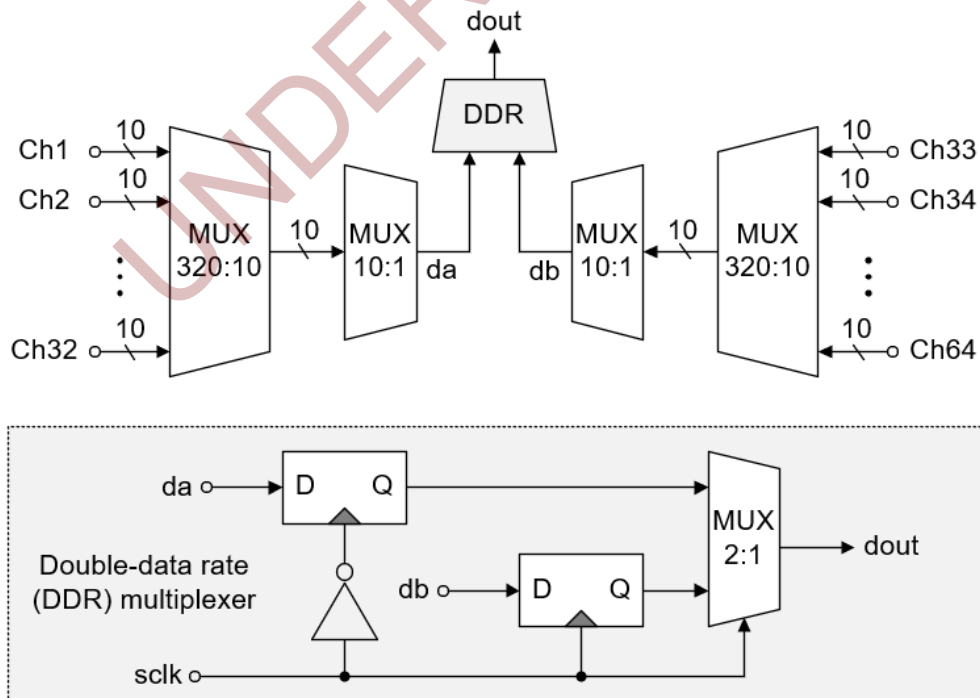

Fig. 9: Digital Serializer block diagram.

Digital data serializer

Two digital data serializers are arranged to facilitate raw data transmission from the 64 recording channels off-chip for testing and debugging purposes. Each of these serializers converts 320 bits from 32 channels into a single bit. Subsequently, a double data rate (DDR) multiplexer converts the resultant 2-line bitstreams ("da" and "db") into a higher frequency (1 MHz) 1-bit bitstream ("dout").

Note that for each serializer, the serialization process has been split into two steps. Firstly, a multiplexer converts 320 bits from 32 channels into 10 bits. Subsequently, in the second step, another multiplexer converts these 10 bits into a single bit. This approach is made for the sake of reuse of the first multiplexer within the feature extraction unit in the digital back-end.

Furthermore, a synchronization signal, denoted as "sync" (not shown in **Fig. 9**), indicates the start of the first channel data transmission. This way, the acquired data can be accurately interpreted and processed by establishing a clear reference point at the outset of data transmission.

Serial Peripheral Interface (SPI)

The digital SPI block includes two main components: a register bank and a serial interface for accessing it. The register bank has 10 addresses, with a maximum of 32 bits of data per address. The serial interface consists of a standard 4-wire slave SPI: chip select (cs), serial clock (sclk), master out slave in (mosi), and master in slave out (miso). Data transmission occurs in synchronization with the clock signal, where data is captured on positive edge of the clock and shifted on negative edge.

There are two types of registers within the register bank: write-read and read-only registers. Write-read registers allow the control of various blocks through their digital interfaces, offering a means to configure their modes of operation. In contrast, read-only registers can only provide a means of monitoring the outputs of these blocks, enabling observation and analysis of their performance.

Moreover, the SPI block includes multiplexed input and output pins, allowing real time monitoring and/or control of specific blocks.

Validation

The majority of the IPs were and will be validated through SPICE simulations across various combinations of supply voltage and manufacturing process corners, targeting the TSMC 40-nm CMOS technology.

Nevertheless, SPICE simulations, while accurate, can be time-consuming to run. For instance, simulating the neural readout channel with its oversampled ADC, which relies on a high-frequency clock signal, requires a significant amount of time. Hence, validating its functionality and performance under many conditions solely through SPICE becomes impractical.

Therefore, we also utilize Veriloga modeling, enabling us to run a large number of tests and validate the functionality and performance of the recording channel through simulations. This approach is considerably faster and less burdensome than SPICE, at the cost of simulation accuracy.

The digital back-end, digital serializer, and SPI block being completely digital, represent an exception and could be fully verified through Verilog simulations. The verification flow consists of three main iterative steps:

1. During the RTL design phase, a testbench was created to verify that all desired functionalities were operating as intended.
2. Following the synthesis of the RTL into gate-level logic, the same testbench used during RTL verification is re-run to confirm that the functionality remains intact when using standard cells;
3. Following the Place and Route (P&R) stage, validations will be performed to ensure timing closure will be achieved. This involves modifying the gate-level netlist to ensure signals arrive at the correct time for seamless chip operation while respecting the timing constraints.

The DBE was extensively validated using prerecorded datasets as reported in [6-7]. **Fig. 10** and **Fig. 11** present the SPICE simulations of the input bias network, while the noise simulation of the front-end OTA

is shown in **Fig. 12**. Furthermore, **Fig. 13** presents the channel simulation in Veriloga, including both functionality and performance evaluation.
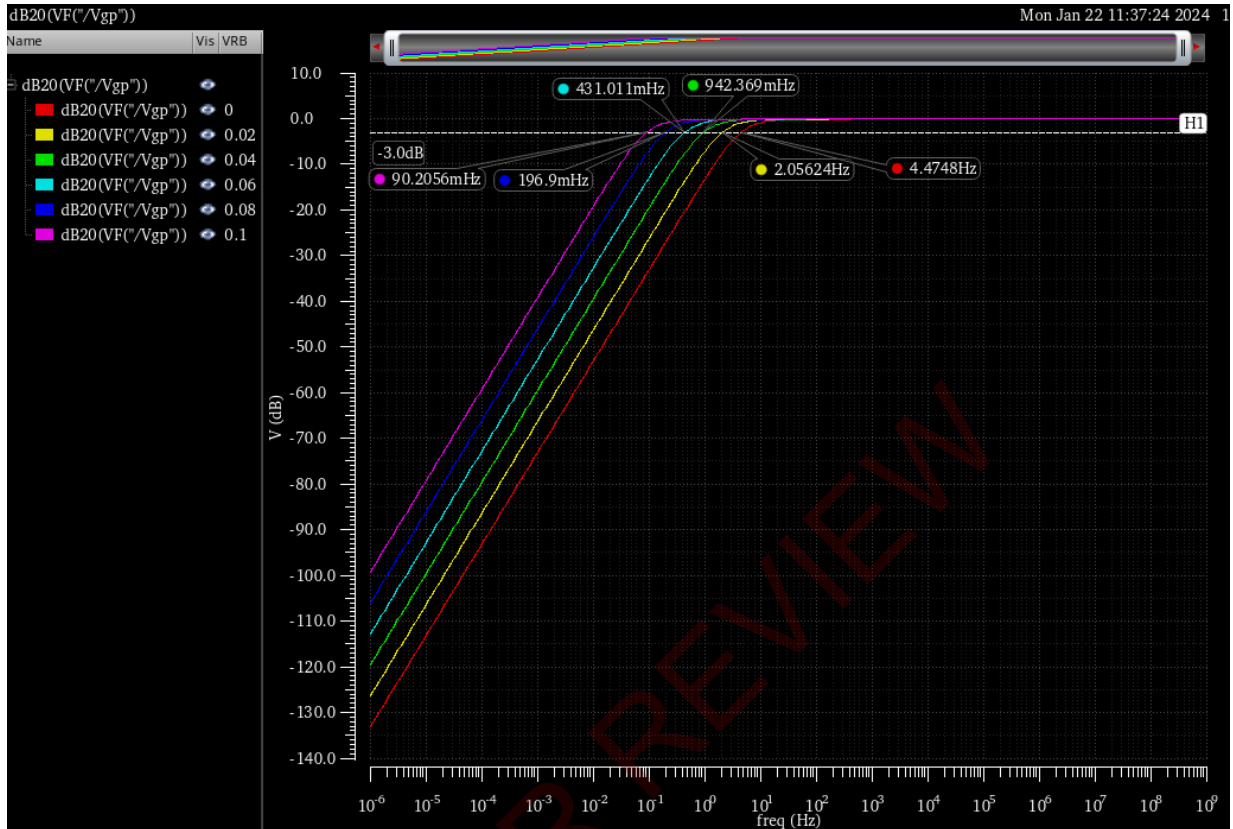

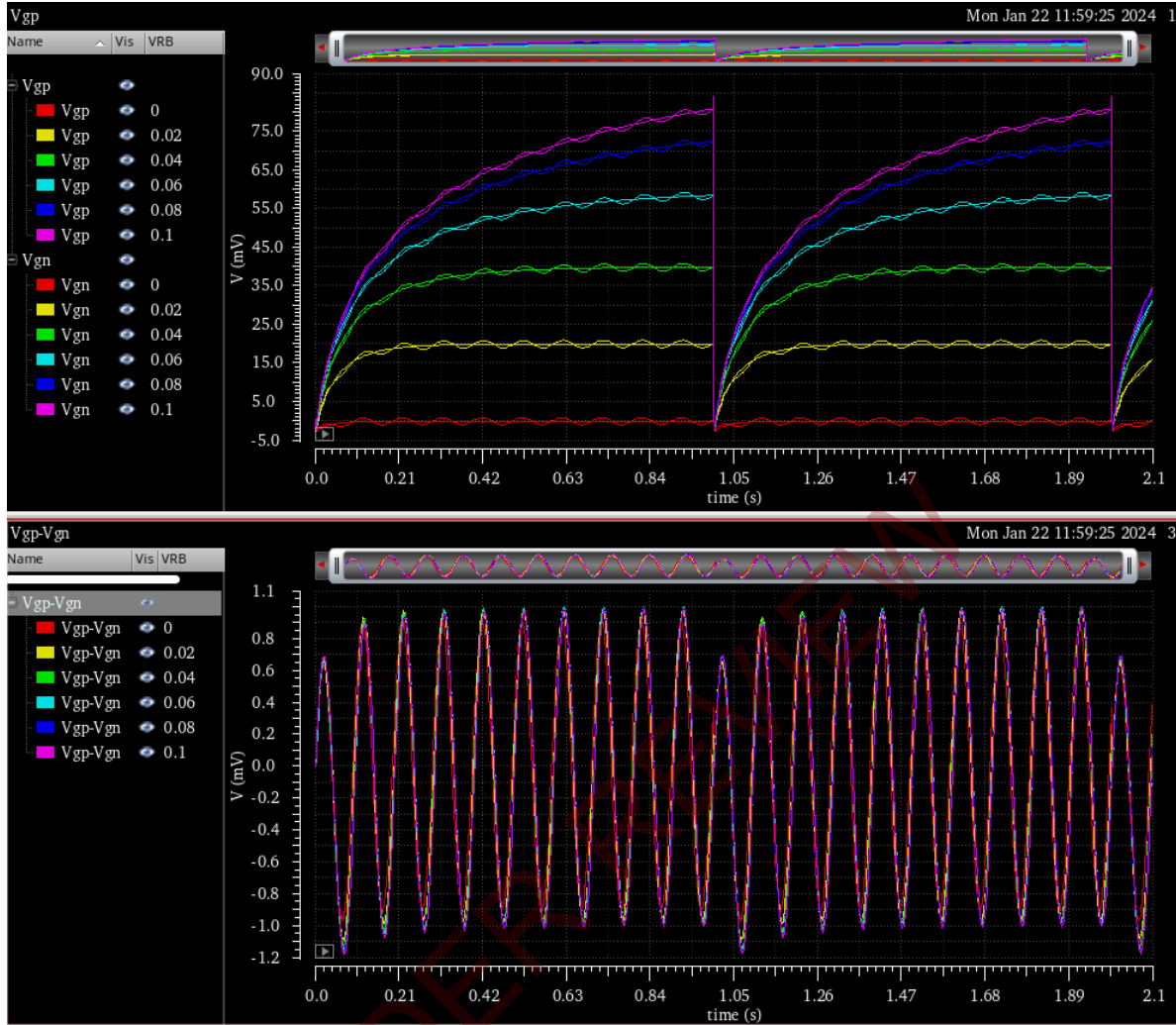**Fig. 10**: AC-simulations of OTA input bias network (switches in OFF state).

Fig. 11: Transient simulations of OTA input bias network with 1-Hz periodic reset.
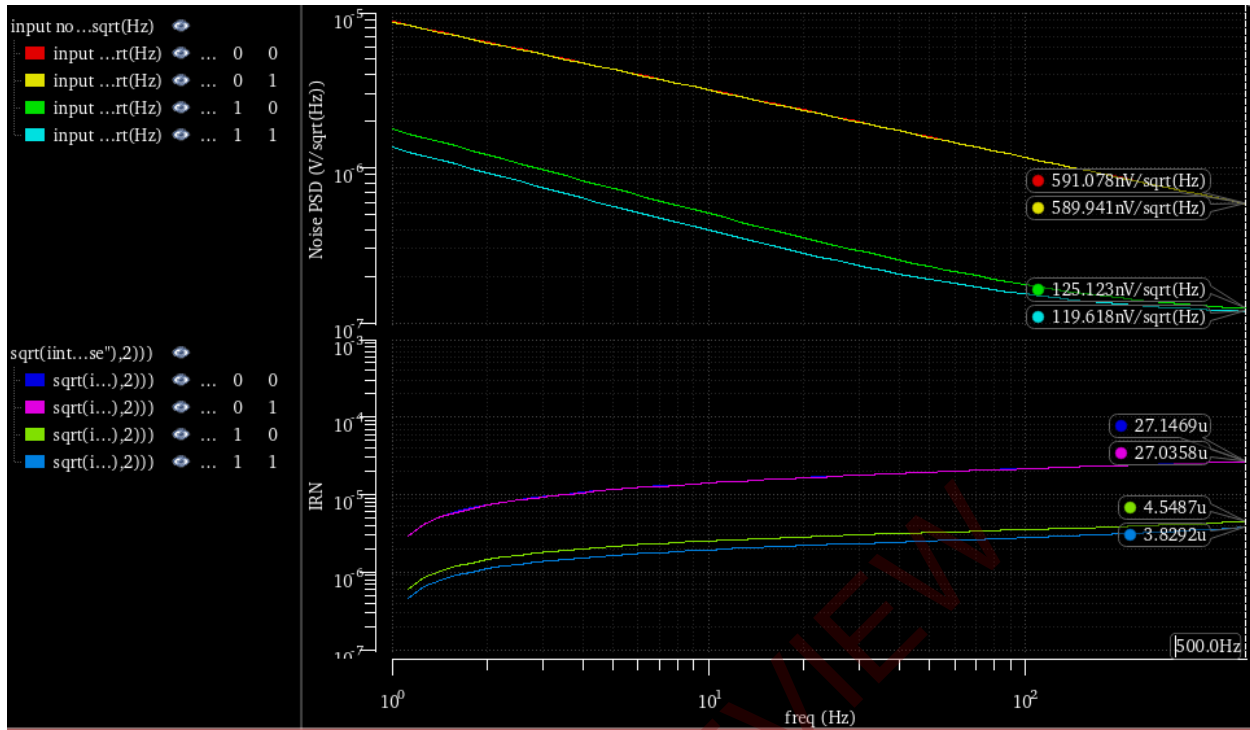
Fig. 12: OTA noise simulations in SPICE, showing that chopping reduces the noise level from 27.1µV to 3.8µV.

Layout and post-layout verification

Following the schematic verification, the fabrication masks will be designed by translating the circuit schematic into a physical layout. The layout will be validated using Calibre Layout Versus Schematic (LVS) and Design Rule Checker (DRC) tools, based on the rules in the Physical Design Kit (PDK) provided by the semiconductor foundry.
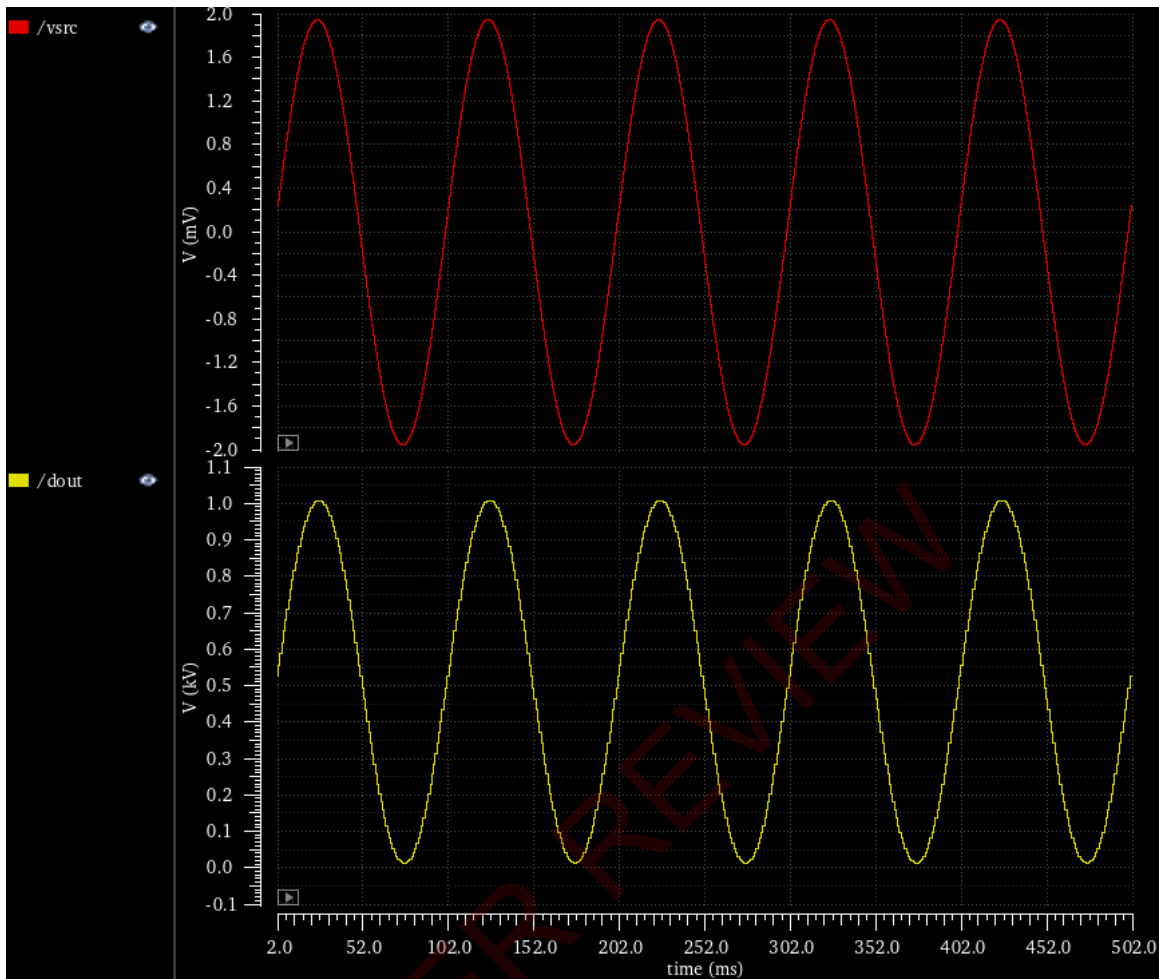
Fig. 13: Simulations of recording channel's functionality and performance (without noise) in Veriloga.

To verify the layout, we will then perform parasitic extraction (PEX) on the recording channel's layout, followed by a rerun of simulations. This step allows us to validate the design under more realistic conditions by including layout dependent effects and parasitics.

Layout of the eREC chip will start in March 2024.

Packaging

Instead of using a commercial package, the eREC chip will be directly wire bonded to a customized printed circuit board (PCB) for full flexibility. This can also reduce the packaging parasitics by removing the connection point between the PCB, package, and the eREC chip.

5. Conclusions

A summary of the progress and future work for the eREC chip is given in **Fig. 14**.

The eREC specifications were specified by the WP1 leader (TUDelft) and a suitable architecture for the physical implementation was defined.

The blocks required for the implementation of the proposed architecture were designed and the recording channel was modelled and validated using Veriloga. In parallel with the system validation, all blocks were designed at transistor level and the corresponding layout will be carried out from March 2024.

The eREC chip is scheduled for fabrication at the end of Q2/2024. Verification of the eREC chips will be carried out in different phases as described in Section 3.

2023			2024										
10_{15}	11	12	1	2	3	4	5_{29}	6	7	8	9	10	11	12
Specification definition			Verification (behavior-level)		Physical design (layout)			PCB design & test			Electrical characterizations		In-vitro & In-vivo validations	
Architecture proposal			Circuit design (sch.)		Verification (post-layout)			Programming for data acq.						
			Verification (schematic-level)		GDS submission			Scripts for data analysis			Chip measurement report			
			Chip design report						Wire-bonding					
			Package design for WB											

Fig. 14: eREC timeline.

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