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Executive Summary

The primary goal of Task 3.2 (Integration of CMOS recording interface and organic neural recording arrays) is to integrate CMOS recording interfaces with organic neural recording arrays, namely passive multi-electrode arrays (MEAs) and ion-gated transistor (IGT) arrays. This deliverable focuses on the optimization of methods for interfacing 64-channel passive MEAs with CMOS platforms developed in WP1. By improving interconnection techniques, we aim to achieve seamless integration without compromising the resolution and accuracy of neural recordings. The initial trials utilized a custom-made anisotropic conductive anisotropic glue, which exhibited variability due to manual application, prompting the shift to automated anisotropic conductive film (ACF) solutions. Through testing and refinement, the two-step ACF bonding process showed significant improvements in connectivity which was evident by spatial maps of impedance values at 1 kHz. The deliverable was completed on time, with no delays or impacts on other project milestones.

1. Introduction

The objectives of WP3 consisted of : (i) Integration of the CMOS recording interfaces with the organic neural recording arrays; (ii) Development of the full EBI by means of biocompatible and flexible interconnections between eFUS and eREC devices. Task 3.2 (Integration of CMOS recording interfaces with the organic neural recording arrays), has been divided into three sub-tasks:

- Optimization of integration technique with PCBs
- Integration of MEA with CMOS recording interface
- Integration of IGT array with CMOS recording interface.

The main results of the above-mentioned sub-task: Optimization of integration techniques with PCBs, entail the content of this deliverable that documents on the integration of CMOS 64-channel recording interface with passive MEA (eREC64).

2. Integration of the CMOS recording interfaces with the organic neural recording arrays

The primary objective of Task 3.2 (Integration of CMOS recording interface and organic neural recording arrays) is to integrate CMOS recording interfaces with organic neural recording arrays. This involves optimizing the methods for interfacing >64-channel passive multi-electrode arrays (MEAs) and ion-gated transistor (IGT) arrays with the CMOS interfaces developed in WP1 (TUD).

2.1. Optimization of integration technique with PCBs

The integration of CMOS recording interfaces with organic neural recording arrays is essential for advancing our research. By combining high-density IGT arrays / passive MEAs with CMOS technology, we aim to significantly improve the resolution and accuracy of neural recordings. This report focuses on optimizing the integration of 64-channel passive MEA interfaces with CMOS interface-compatible contacts. The optimized technique will serve as a foundation for integrating various types of probes with the CMOS interface. The proposed process relies on precision alignment through flip-chip technology, ensuring high-performance bonding. The progress made in establishing reliable interconnections between organic electronics neural probes and the CMOS interface compatible contacts have been done in collaboration with TUD.

To evaluate the quality of interconnections, we connected various probes to a commercially available electrophysiology acquisition system. We selected the Open Ephys acquisition system for its ease ofuse, ability to measure impedance at 1 kHz, reliability, and affordability. This system includes an acquisition board capable of streaming up to 512 channels of neural data to a computer via USB, along with a low-profile 64-channel headstage equipped with a 3-axis accelerometer, based on the INTAN RHD2164 chip.

The upper side of the headstage houses the SPI connector for connecting the SPI cable to the acquisition board, while the lower side holds the RHD2164 chip and a male HIROSE EIB connector for interfacing with the neural probe. To facilitate the connection to this headstage, we designed several PCB board adaptors. One side of each adaptor connects to our neural probe, and the other side accommodates a female HIROSE EIB connector to interface with the headstage (**Figure 1.1C**). This design allows us to attach multiple neural probes to our adaptors, enabling seamless testing with the headstage.

For connecting the neural probes to the PCB board adaptor, we chose a BGA (Ball Grid Array) package-like contact format, as it is commonly used in INTAN RHD2164 chips and other similar applications, and could simplify future integration with our custom chip (**Figure 1.1B**). Consequently, we designed both the backside of our PCB adaptor and our microfabricated neural probes with BGA contacts, allowing them to be securely attached. The connection was made using flip-chip bonding, a method we plan to use for interfacing with our custom chip in future iterations (**Figure 1.1D**). The final assembled connection is shown in Figure 1.1E.

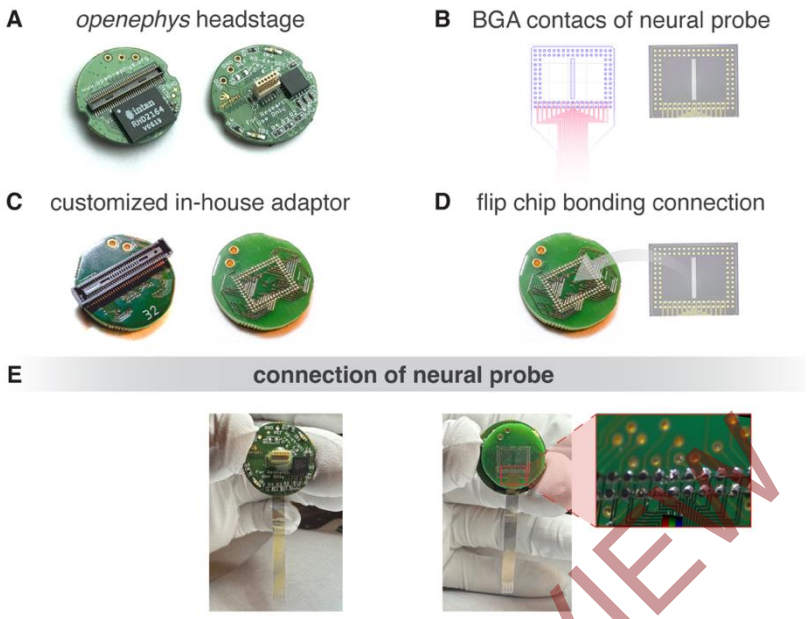

Figure 2-1 : Connectors and connection strategy

In our initial trials, we used a custom-made conductive anisotropic glue composed of organic materials (PEDOT:PSS, chitosan, d-sorbitol). This glue was chosen for its conductive properties, ease of application, and low production cost allowing us to establish manual interconnections. However, due to the reliance on human precision, we experienced variability in the performance of specific arrays.

Figure 1.2 shows the impedance map of the probe after packaging with the conductive glue. While connections were successfully made, the impedance data reveals inconsistent values across the device, likely due to uneven glue distribution and imperfect contact between the MEA and the PCB board. These inconsistencies highlighted the limitations of manual application, prompting us to seek a more controlled and automated integration method.

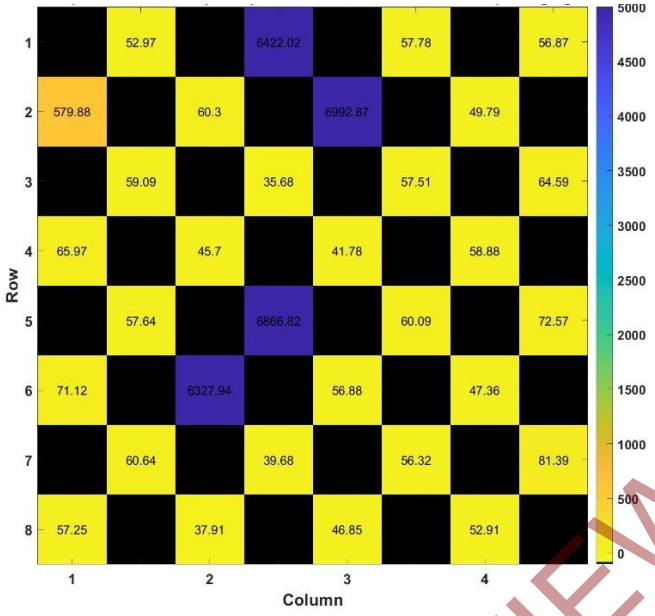

Figure 2-2: : Impedance map (in kΩ) of a 32-electrode array measured using custom made anisotropic conductive glue. The color scale indicates impedance values across the 8x4 grid, with most electrodes showing low impedance (yellow) and a few high-impedance regions (blue) above 6000 kΩ.

To improve the reliability and precision of the interconnections, we turned to commercially available anisotropic conductive films (ACF). ACFs offer several advantages over our custom-made anisotropic conductive glue, as they come in pre-fabricated films with uniformly spaced conductive particles of specified size. This structured composition allows for the use of automated bonding machines, resulting in improved alignment precision and consistent conductivity.

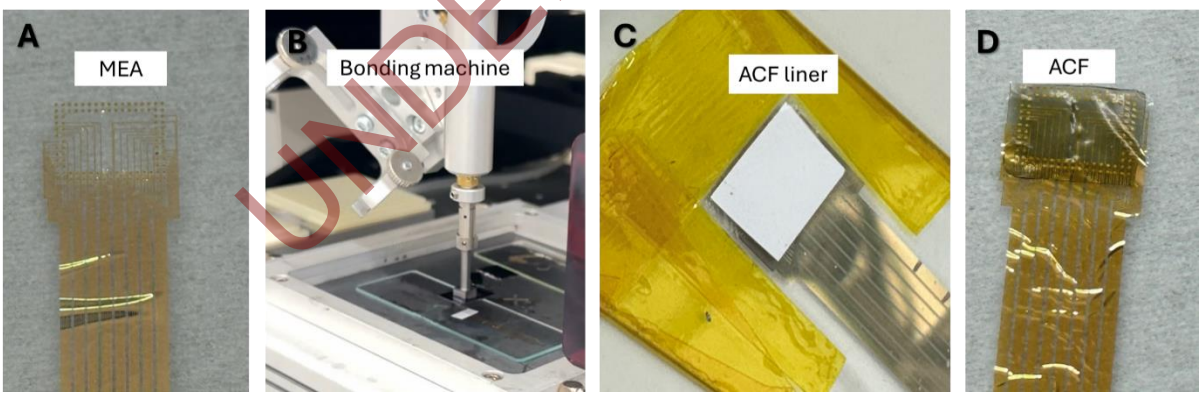

Figure 2-3: (A) Image of the back-end of a multi-electrode array (MEA) before bonding. (B) Bonding process using a precision machine to align and apply pressure for attaching the PCB and MEA using anisotropic conductive film (ACF). (C) Anisotropic conductive film (ACF) liner, shown prior to bonding, which is removed during the process to expose the adhesive. (D) Final image of the MEA after bonding with ACF, showing the successful attachment to the PCB for further testing and use.

The first commercially available ACF we tested was 3M™ ACF 9703 with a medium pitch of 50 µm. A small piece of the ACF was cut and placed over the BGA contacts on the back-end of the probe. For the bonding process, we used the Tresky 3000- PRO bonding machine, which is equipped with a split-camera system for precise alignment between the MEA and the PCB (**Figure 1.3B**). The split-camera allowed us to simultaneously view both components, ensuring the alignment marks on the PCB and MEA were matched with a precision of approximately 1 µm. Once aligned, a pressure of 1 kg was applied to ensure proper adhesion between the two elements. No heat was applied during this initial test to assess the performance of the ACF at room temperature (**Figure 1.4**).

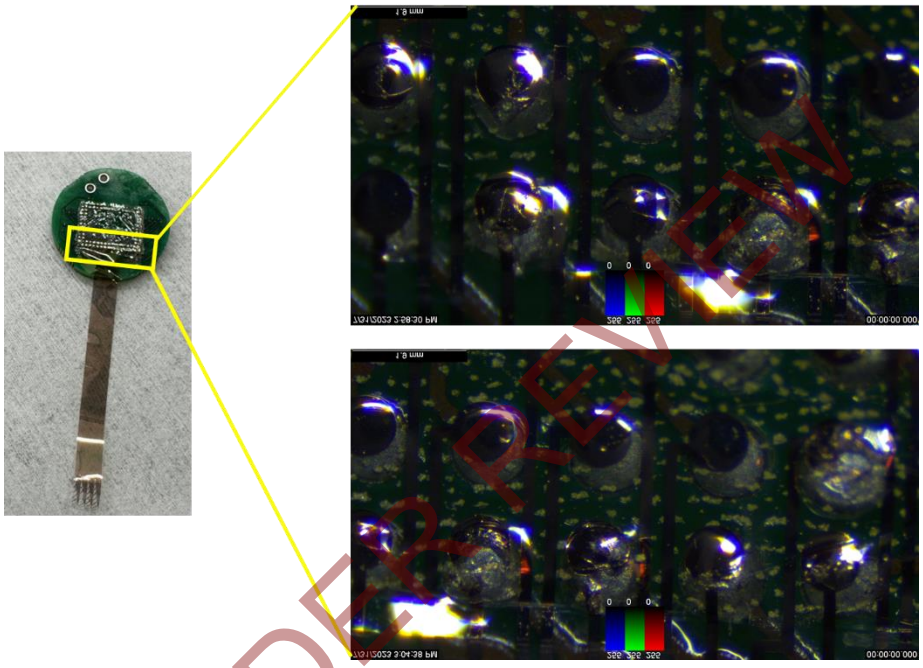

Figure 2-4: Image of MEAs connected using the first anisotropic conductive tape. The zoomed-in sections display the contact points between the flexible PCB and the probe, highlighting the quality of the electrical connections made using the anisotropic conductive film (ACF) technology. The ACF process shown here involved applying pressure without heating, as part of the initial trials to test bonding efficacy.

Figure 1.5 displays a spatial map of the electrodes with their corresponding impedance values at 1 kHz after ACF bonding. The high impedance observed across most electrodes indicates that the quality of the interconnections was insufficient for high SNR neural recordings. This suggests that the conductive particles within the ACF did not form a uniform vertical conductive pathway, likely due to factors such as insufficient pressure, lack of heat, or a low density of conductive particles relative to the density of our contacts. Further tests with this specific ACF, even with added heat and increased pressure, did not yield better results. Considering these limitations and the restricted spatial resolution due to the low particle density in the ACF, we moved on to testing another commercially available ACF.

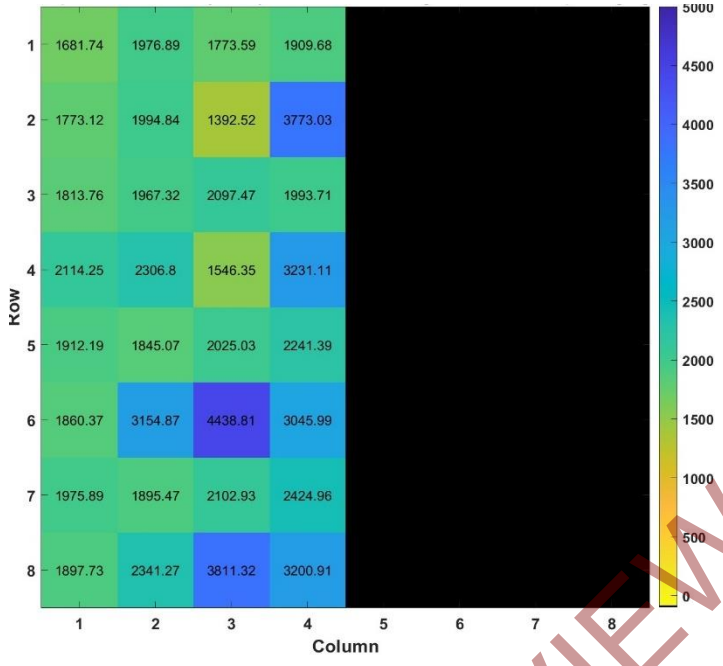

Figure 2-5: Impedance map (in kΩ) of a 32-electrode array measured after packaging using 3M™ ACF 9703. The color scale indicates impedance values across the 8x4 grid, with most electrodes showing impedance between 1000-3000 kΩ.

To address the issues observed with the 3M™ ACF 9703 test, we tested TFA22023-30, with a pitch of 800 µm with various bonding protocols. Among the various protocols, we found that a two-step approach was the most efficient.

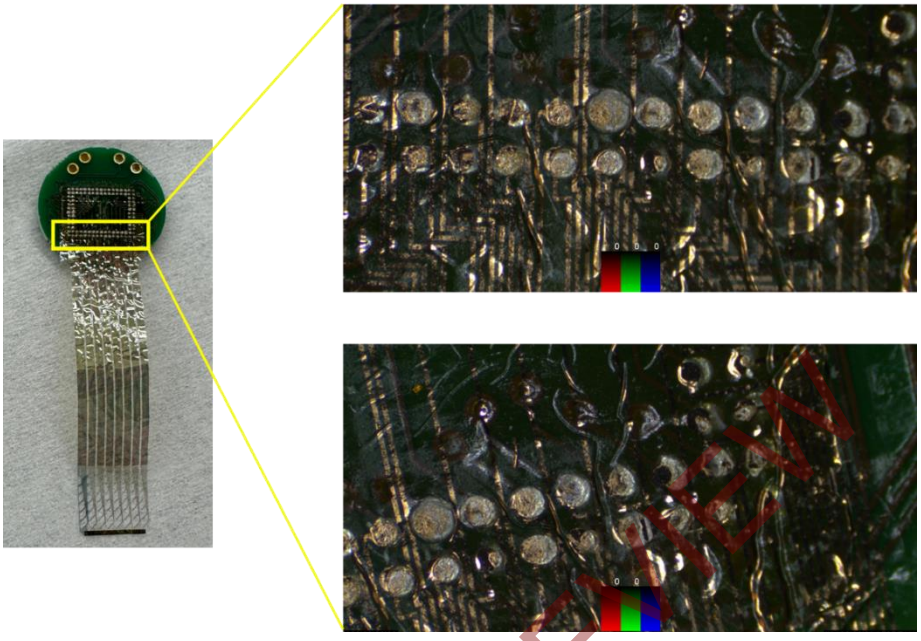

Figure 2-6: Image of the MEAs probe after assembly, with close-up views of the connection points. The zoomed-in images highlight the quality of the electrical connections between the flexible probe and the PCB using anisotropic conductive film (ACF) technology. The close-ups show the alignment and contact points, where the conductive particles create the electrical pathway, ensuring proper signal transmission. These images are essential for verifying the integrity of the connections after the packaging process.

During that approach, the first step involved applying a pressure of 1 kg at 80°C for 5 seconds, followed by a second step where we increased the pressure to 30 kg and the temperature to 160°C, maintaining these conditions for another 30 seconds. This combination of heat and pressure was designed to ensure that the conductive particles within the ACF created a uniform and stable conductive pathway between the MEA and the PCB interface. **Figure 1.6** shows microscope images of the probe after lamination using this refined ACF protocol. The impedance measurements taken after the lamination show significantly improved performance, with impedance values lower and more consistent across the device compared to the earlier trials.

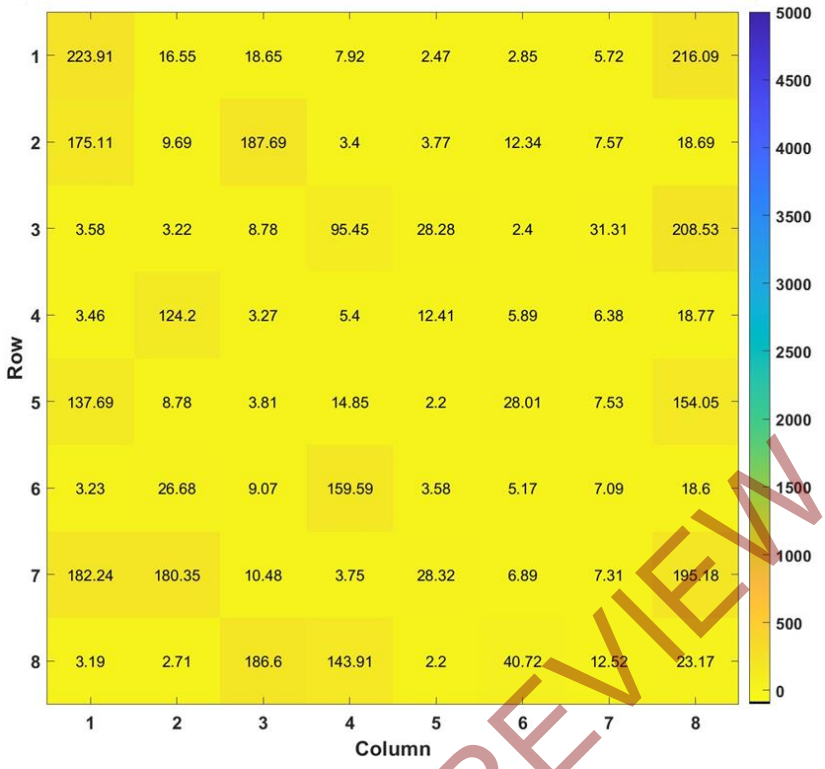

Figure 2-7: Impedance map (in kΩ) of 64 electrodes across an 8x8 grid after packaging using ACF TFA22023-30. The color scale represents impedance values, with most electrodes showing low impedance, indicating successful electrical connections across the majority of the grid.

Following the successful packaging of the device using the refined ACF protocol, we conducted a comprehensive impedance analysis to evaluate the performance of the connections. As shown in **Figure 1.7**, the impedance map indicates that the device achieved stable and low impedance across all channels, confirming the effectiveness of the optimized ACF integration technique. These results are promising for the integration of both MEAs and IGT arrays with the CMOS recording interface, as they demonstrate the reliability of the interconnections and the suitability of TFA22023-30 technology for this application.

3. Conclusions

We successfully integrated organic electronics neural arrays with a test PCB featuring BGA contacts, using methods and materials proven compatible with our CMOS technology. After initial challenges with manual conductive glue applications, the introduction of anisotropic conductive films (ACF) enabled more precise and reliable interconnections. Refining the bonding protocols, particularly using the two-step bonding process, led to stable, low-impedance connections across all channels. This optimization has demonstrated the suitability of ACF technology for integrating both MEAs and IGT arrays with CMOS platforms, paving the way for future high-resolution, low-noise neural recordings. The project remains on schedule, and the progress made provides a solid foundation for further testing and integration efforts.